1.6T OSFP DR8/2xDR4 Optical Transceiver

Features

- Hot-pluggable 1.6T OSFP-RHS 2xDR4 form factor
- Dual MPO-12 APC receptacles or Single MPO-16 APC receptacles
- Silicon photonics MZM solution
- 8x106.25GBd PAM4 electrical and optical interface
- Maximum link length of 500m G.652 SMF fiber
- Operating case temperature 0°C to +70 °C
- Power dissipation < 26W
- Compliant with RoHS 2.0

Standards Compliance

- IEEE802.3dj
- OSFP MSA

Applications

- Data center and cloud networks
- InfiniBand XDR

General Description

Trilight OSFP optical module is designed for 1.6Tbps Ethernet links and supports 500 meters of single-mode fiber transmission. The module features 8 independent electrical I/O channels, each with a maximum rate of 212.5Gbps.The tranceiver operates at central wavelengths of 1311nm.

The module's transmit path integrates an 8:8 PAM4 retimer with a high-swing output driver, connected externally to a Silicon photonics MZM and continuous-wave laser. The receive path includes two 4-channel PD and TIA arrays, also integrates PAM4 retimer.

The module's electrical interface complies with the IEEE 802.3dj-defined 1.6TAUI-8 standard and follows the OSFP MSA packaging specification.

Part No.	Specifications					
	Package	Data rate	Wavelength	Temp	Reach	Optical Interface
VD6R5-K031C	OSFP-RHS	1.6Tbps	1311±6.5nm	0~70℃	500m	1*MPO16
VD6R5-J031C	OSFP-RHS	1.6Tbps	1311±6.5nm	0~70℃	500m	2*MPO12

1 Absolute Maximum Ratings and Operation Conditions

Table 1.1 Absolute Maximum Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit
Storage temperature	TS	-40		+85	℃
Case Operating Temperature	TOP	0		70	℃
Maximum Supply Voltage	Vcc	-0.5		4	V
Relative humidity	RH	5		85	%
Receiver Damage Threshold per lane	Pdamg	5			dBm

Table 1.2 Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Operating case temperature	Tc	0		70	℃	
Power supply voltage	Vcc	3.135	3.3	3.465	V	
Power dissipation	PD			26	W	
Supply Current	Icc			8.29	A	
Electrical signal rate per channel (PAM encoded)			106.25		GBd	
Optical signal rate per channel (PAM encoded)			106.25		GBd	
Power supply noise				66	mVpp	
Pre-FEC Bit Error Ratio				2.4x10-4		
Post-FEC Bit Error Ratio				1x10-12		
Receiver differential data output load		100			Ω	
Fiber length (9um SMF)		2		200	m	

2 OSFP Parameters

2.1 OSFP Electrical Pin Assignment

The OSFP module is based on a 60 pin electrical connector with pin out as specified in OSFP Hardware specification. The 60 electrical pins allow exchanging high speed data, control and alarm signals between module and host board. The pin-outs are summarized below：

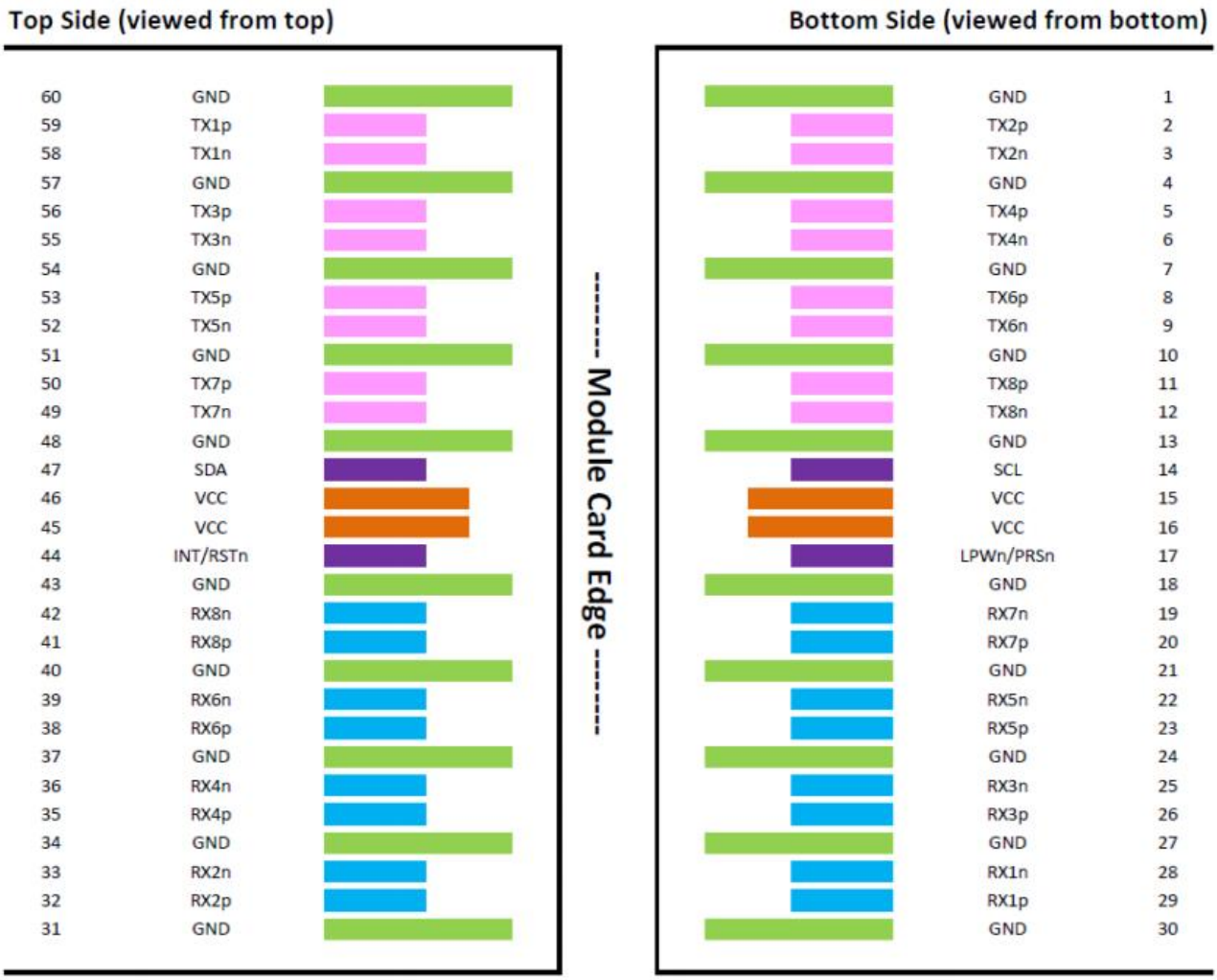

Figure 2.1 OSFP module pinout

Pad#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
1	GND	Ground				
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	nput from Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	nput from Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground			1	
8	TX6p	Transmitter Data Non-Inverted	CML-I	nput from Host	3	
9	TX6n	Transmitter Data Irverted	CML-I	nput from Host	3	
10	GND	Grounc			1	
11	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX6n	Transmitter Data Inverted	CML-I	nput from Host	3	
13	GND	Ground				
14	SCL	2-wire serial interface clock	LVCMOS-VO	Bi-directional	3	Open-Drain with pull-up resistor on Host
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/PRSn	Low-Power Mode/Module Present	Multi-Level	Bi-directional	3	See pin description for reguired circ uit
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground				
22	RX5n	Receiver Data Irverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Irverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
27	GND	Ground				

28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
30	GND	Ground				
31	GND	Ground				
32	RX2p	Receiver Data Non-Irverted	CML-O	Output to Host	3	
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Irverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
39	RX6n	Receiver Data Irverted	CML-O	Output to Host	3	
40	GND	Ground				
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3	
43	GND	Ground				
44	INT/RSTn	Module Interrupt/Module Reset	Multi-Level	Bi-directional	3	See pin description for required circuit
45	VCC	+3.3V Power		Power from Host	2	
46	VCC	+3.3V Power		Power from Host	2	
47	SDA	2-wire serial interface Data	LVCMOS-VO	Bi-directional	3	Open-Drain with pull-up resistor on Host
48	GND	Ground				
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3	
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
51	GND	Ground				
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3	
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
54	GND	Ground				
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3	

56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground				
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-1	Input from Host	3	
60	GND	Ground				

2.2 OSFP Electric Ports Definition

Parameter	Symbol	Unit	Min	Typ	Max	Note
Power Supply Current	Icc	mA			8290	
Transceiver power consumption	P	W			26	
AC coupling capacitors (Internal)		nF		100		
Transmitter						
Signaling rate per lane		GBd		106.25		
Differential peak-peak voltage Output enabled Output disabled		mV			1200 30	
AC common-mode peak-to-peak voltage Low-frequency, VCMLF Full-band, VCMFB		mV			15 60	
DC common-mode voltage		mV	0.15		1.05	
Effective return loss	ERL	dB	8.5			
Common-mode to common-mode return loss	RLcc(min)	dB	Equation(179–12)			
Common-mode to differential -mode return loss	RLcc(min)	dB	Equation(179–13)			
Transmitter steady-state voltage,	v_f	V	0.4		0.6	
Linear fit pulse peak ratio	R_{peak}		0.55			
Level separation mismatch ratio	R_{LM}		0.95			
Signal-to-noise-and-distortion ratio	SNDR	dB	30			
Signal-to-residual-intersymbol-interference ratio, SNRISI Output		dB	28			
Jitter J_{RMS03} EOJ_{03} $J4u_{03}$		UI			0.023 0.025 0.118	
Receiver						
Signaling rate per lane		GBd		106.25 ± 50 ppm		

Single-ended voltage tolerance range		V	-0.4		1.4	
DC common-mode voltage tplerance		V	0.15		1.05	
AC common-mode peak-to-peak voltage Low-frequency, VCMLF Full-band, VCMFB		mV			32 80	
Common-mode to common-mode return loss	RLcc(min)	dB	Equation (179–12)			
Common-mode to differential-mode return loss	RLdc(min)	dB	Equation (179–13)			
Differential termination mismatch		%			10	
Amplitude tolerance		V		0.5		
Interference tolerance			Table 176D–10			
Jitter tolerance			Table 176D–11			

2.3 Optical Characteristics

Parameter	Symbol	Unit	Min	Typ	Max	Note
Transmitter						
Signaling speed per lane		GBd		106.25		
Signaling Speed Tolerance		ppm	-50		+50	
Modulation Format		PAM4				
Lane Wavelength		nm	1304.5	1311	1317.5	
Side Mode Suppression Ratio	SMSR	dB	30			
Average TX Power	Pavg	dBm	0		4	a,b
Outer Optical Modulation Amplitude for TDECQ < 1.4dB for 1.4dB ≤ TDECQ ≤ 3.4dB	OMAouter	dBm	 -0.1 -1+TDECQ		4.2	
Extinction Ratio	ER	dB	3.5			
Average launch power of OFF transmitter, each lane	Poff	dBm			-15	

Transmitter and dispersion eye closure for PAM4	TDECQ	dB			3.4	
Transmitter eye closure for PAM4	TECQ	dB			3.4	
|TDECQ - TECQ|		dB			2.5	
Transmitter overshoot and undershoot		%			22	
Total average launch power		dBm			10	
Transmitter transition time		ps			8	
RIN17.1 OMA	RIN	dB/Hz			-139	
Optical return loss tolerance	ORTL	dB			21.4	
Transmitter reflectancee		dB			-26	c
Receiver						
Signaling Speed		GBd		106.25		
Signaling Speed Tolerance			-50		+50	
Modulation Format		PAM4				
Lane Wavelength	λ_C		1304.5	1311	1317.5	
Damage threshold, each lane		dBm	5			d
Average receive power each lane	Rx_{AVG}	dBm	-6.1		4	e
RX Power (OMA_{outer})	Rx_{OMA}	dBm			4.2	
Receiver reflectance		dBm			-26	
Receiver sensitivity (OMAouter), each lane for TECQ < 0.9 dB for 0.9 dB < TECQ < SECQ	Sen_{OMA}	dBm			-3.4 -3.4+TECQ	
Stressed receiver sensitivity (OMAouter),each lane		dBm			-0.9	f
Conditions of Stressed RX Sensitivity Test						
Stressed eye closure for PAM4 (SECQ),lane under test	SECQ	dB	3.4			g
OMA_{outer} of each aggressor lane		dBm	4.2			h
LOS Assert	LOSA	dBm	-15			

LOS De-Assert	LOSD	dBm			-8.4	
LOS hysteresis		dB	0.5			

Notes:

a. Average launch power, each lane (min) is not the principal indicator of signal strength. A transmitter with launch power
below this value cannot be compliant; however, a value above this does not ensure compliance.

b. An average launch power of –3.3 dBm corresponds to an OMA of –0.3 dBm with an infinite extinction ratio.

c. Transmitter reflectance is defined looking into the transmitter.

d.The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level. The receiver does not have to operate correctly at this input power.

e. Average receive power, each lane (min) is not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

f. Measured with conformance test signal at TP3 (see 180.8 in IEEE 802.3dj) for the block error ratio specified in 180.2.

g.These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

h.No aggressors needed for 200GBASE-DR1 in a single lane device.

2.4 Digital Diagnostic Functions

Parameter	Symbol	Min	Max	Units	Notes
Temperature monitor absolute error	DMI_Temp	-3	3	℃	Over operating temperature range
Supply voltage monitor absolute error	DMI _VCC	-0.1	0.1	V	Over full operating range
Channel RX power monitor absolute error	DMI_RX_Ch	-2	2	dB	
Channel Bias current monitor	DMI_Ibias_Ch	-10%	10%	mA	
Channel TX power monitor absolute error	DMI_TX_Ch	-2	2	dB	

2.5 Recommended Power Supply Filter

Figure 2.2 provides an example implementation for a 3.3V power filter on the host board. If an alternate circuit is used for power filtering then the same filter characteristics as this example filter shall be met.

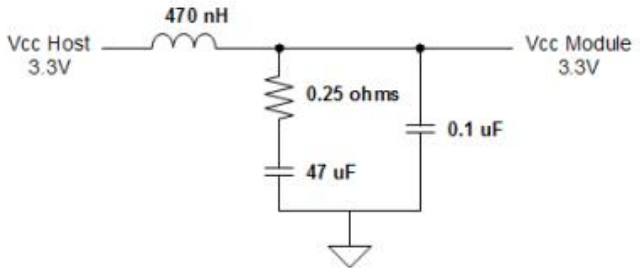

Figure 2.2 Recommended Host Board Power Supply Filtering

2.6 OSFP Host Board and Module Block Diagram

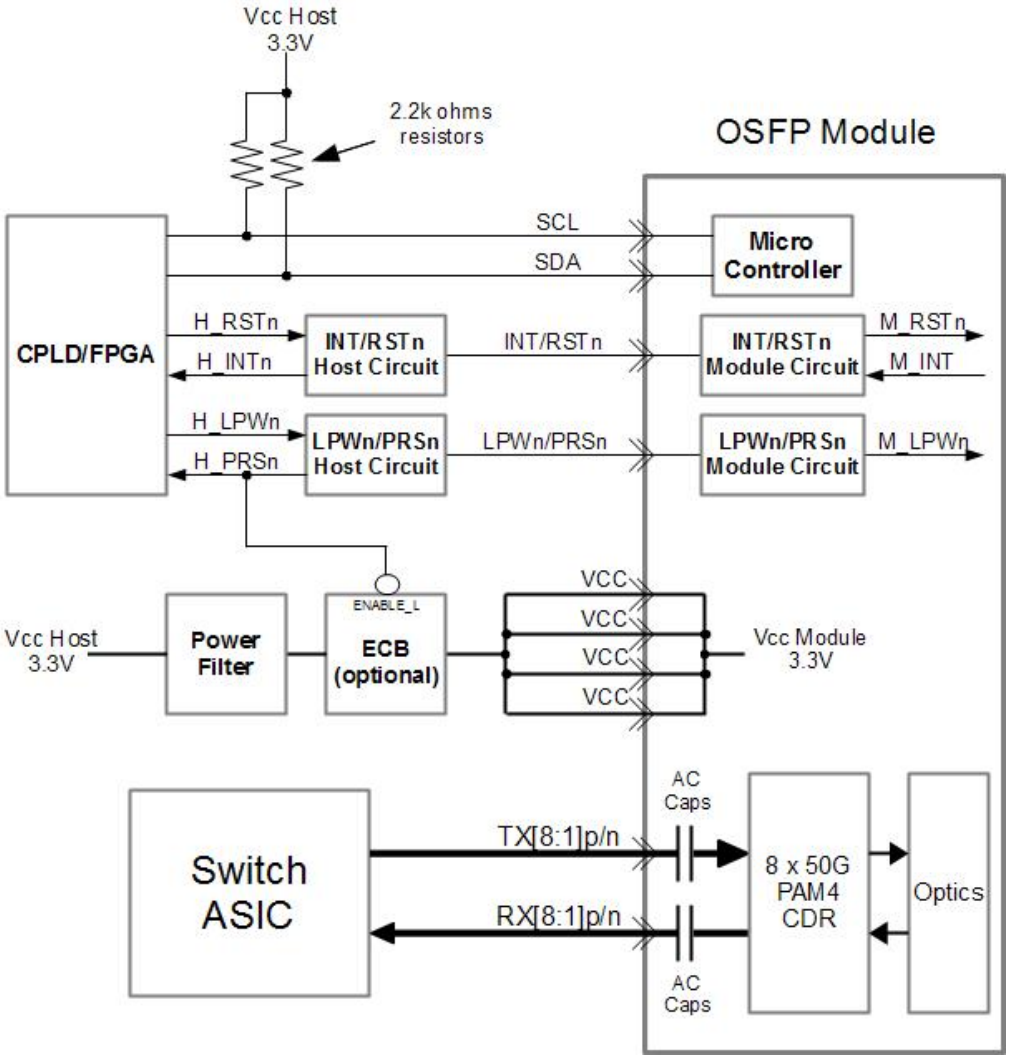

Figure 2.3 OSFP Host Board and Module Block Diagram

2.7 Module Memory Map

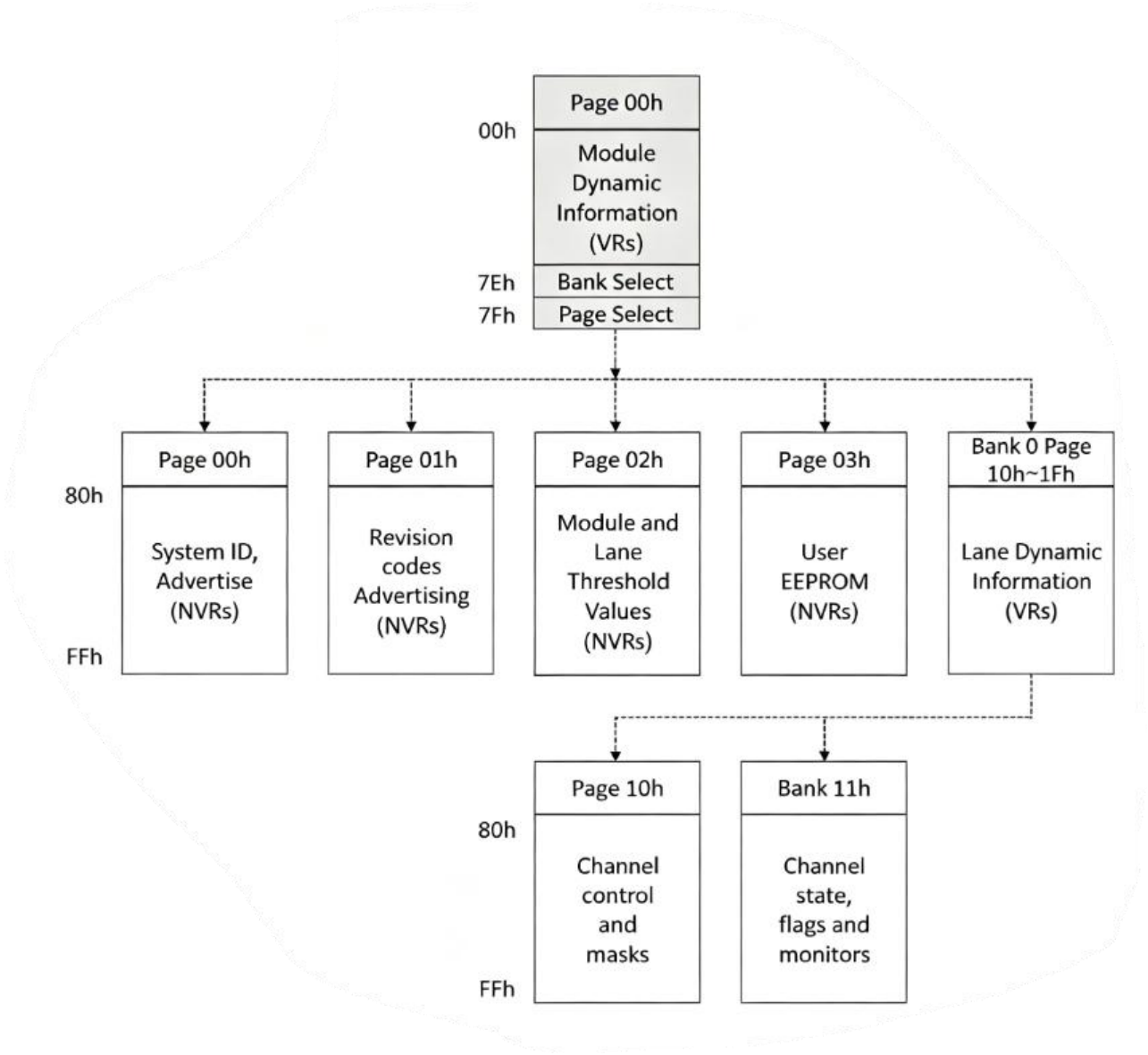

Figure 2.4 Simplified OSFP CMIS Module Memory Map Architecture

3 Environment Regulation Compliance and product Safety

Category	Standard
Radiated Emissions	EN 55032 Class B CISPR 32 Class B FCC rules 47 CFR Part15
Radiated Immunity	EN 55035 CISPR 35 IEC/EN 61000-4-3
RoHS	EU RoHS 2.0 (2011/65/EU) REACH (EC 1907/2006) China RoHS SJ/T 11363
Laser Safety	IEC 60825-1:2014+A11:2021 FDA/CDRH Class 1 Laser Product, 21 CFR 1040.10 & 1040.11
ESD	IEC 61000-4-2； ANSI/ESDA/JEDEC JS-001； MIL-STD-883C Contact ±8kV, Air ±15kV
Flammability (PCB)	UL Class 94 V-0
Reliability	GR-468-CORE、IEC 61300-2

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5 Revision History

Revision	Date	Description
V1.0	2026.5.10	Advance Release.