## Features

- Hot-pluggable OSFP Riding Heat Sink form factor
- Maximum link length of 100m on OM4 fiber with FEC
- +3.3V single power supply
- Power dissipation < 9W
- Operating case temp Commercial: 0°C to +70 °C
- MPO-12 APC connector
- RoHS compliant

## Applications

- 400GBASE-SR4 400G Ethernet
- Breakout to 2x200G Ethernet
- Breakout to 4x100G Ethernet

## Order Information

**Table 1-Order Information**

| Product | Bit Rate (Gbps) | Laser (nm) | Distance note1 | Fiber Type | DDMI | Connector | Temp note2 |
|---|---|---|---|---|---|---|---|
| 400G OSFP SR4 | 425.0 | 850 | 100m | MMF | YES | MPO 1x12 APC | 0℃~+70℃ |

Note:
1. OM4 fiber, 60m for OM3 fiber, with FEC; For 100m OM4 version, please contact us.
2. Case Temperature

## Absolute Maximum Ratings

**Table2- Absolute Maximum Ratings**

| Parameter | Symbol | Min. | Typical | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| Supply Voltage | $Vcc_3$ | -0.5 | - | +3.6 | V | |
| Storage Temperature | $T_s$ | -40 | - | +85 | °C | |
| Operating Humidity | RH | +5 | - | +85 | % | 1 |
| Control Input Voltage | VI | -0.3 | - | VCC+0.5 | V | 1 |

Note:1 No condensation

## Recommended Operating Conditions

**Table 3- Recommended operating Conditions**

| Parameter | Symbol | Min. | Typical | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| Operating Case Temperature | $T_C$ | 0 | - | +70 | °C | |
| Power Supply Voltage | Vcc | 3.135 | 3.3 | 3.465 | V | |
| Power Dissipation | Pd | - | - | 9 | W | |

## Electrical Characteristics

**Table 4- Electrical Characteristics**

| Parameter | Symbol | Unit | Min | Typ | Max | Notes |
|---|---|---|---|---|---|---|
| **Transmitter** | | | | | | |
| Signaling Rate per Lane | SR | Gbd | 53.125 ± 100 ppm | | | 1 |
| Modulation format | - | - | PAM4 | | | |
| Differential pk-pk voltage tolerance | Vin,pp,diff | mV | 750 | | | |
| Differential termination mismatch | - | % | | | 10 | |
| Single-ended voltage tolerance range | - | V | -0.4 | | 3.3 | |
| DC common-mode voltage tolerance | - | V | -0.35 | | 2.85 | |
| **Receiver** | | | | | | |
| Signaling Rate per Lane | SR | Gbd | 53.125 ± 100 ppm | | | 1 |
| Modulation format | - | - | PAM4 | | | |
| Differential peak-to-peak output voltage (Short mode) | | mV | | | 600 | |
| Differential peak-to-peak output voltage (Long mode) | | mV | | | 845 | |
| Transition time (20% to 80%) | tr, tf | ps | 8.5 | | | |
| Eye height | EH | mV | | | 15 | |
| Vertical eye closure, | VEC | dB | | | 12 | |
| Differential termination mismatch | | % | | | 10 | |
| DC common-mode voltage tolerance | | V | -0.35 | | 2.85 | |

**Table 5-Optical Characteristics**

| Parameter | Symbol | Unit | Min | Typ | Max | Notes |
|---|---|---|---|---|---|---|
| **Transmitter** | | | | | | |
| Center wavelength | CW | nm | 840 | | 868 | |
| RMS Spectral Width | SW | dBm | - | - | 0.6 | |
| Average Launch Power per Lane | AOP | dBm | -4.6 | | 4 | |
| Outer Optical Modulation Amplitude (OMAouter), each lane | OMA | dBm | − 2.6 | | 3.5 | 2 |
| | | | − 4.4 + max (TECQ, TDECQ) | | | 3 |
| Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane | TDECQ | dB | | | 4.4 | |
| Transmitter eye closure for PAM4 (TECQ), each lane | TECQ | dBm | | | 4.4 | |
| Transmitter power excursion, each lane | TPE | dB | | | 2.3 | |
| Optical Extinction Ratio | ER | dBm | 2.5 | | | |
| Transmitter transition time, each lane | Tt | | | | 17 | |
| RIN14OMA | | | | | − 132 | |
| Optical Return Loss Tolerance | ORL | | | | 14 | |

| | | | | | | |
|---|---|---|---|---|---|---|
| Encircled Flux | FLX | | >86% at 19 um<br><30% at 4.5 um | | | |
| Average Launch Power of OFF Transmitter, per Lane | | | | | -30 | |
| **Receiver** | | | | | | |
| Wavelength | W | nm | 840 | 850 | 948 | |
| Damage Threshold | | dBm | 5 | | | |
| Average Receive Power per Lane | DT | dBm | -6.4 | | 4 | |
| Receive power, each lane (OMA outer) | RXPx | dBm | | | 3.5 | |
| Receiver Reflectance | RxOMA | dB | | | -15 | |
| LOS Hysteresis | Rfl | dB | 0.5 | 1 | | |
| Receiver sensitivity (OMA outer) | RxSen | | | | - 4.6 | 2 |
| | | | | | - 6.4 + TECQ | 3 |

**Note:**

1. **Transmitter consists of 4 lasers operating at a maximum speed of 53.125 ± 100ppm Gbaud each;**
2. **For max (TECQ, TDECQ)≤1.8 dB;**
3. **For 1.8 ≤ max (TECQ, TDECQ) ≤ 4.4 dB;**

## Recommended Interface

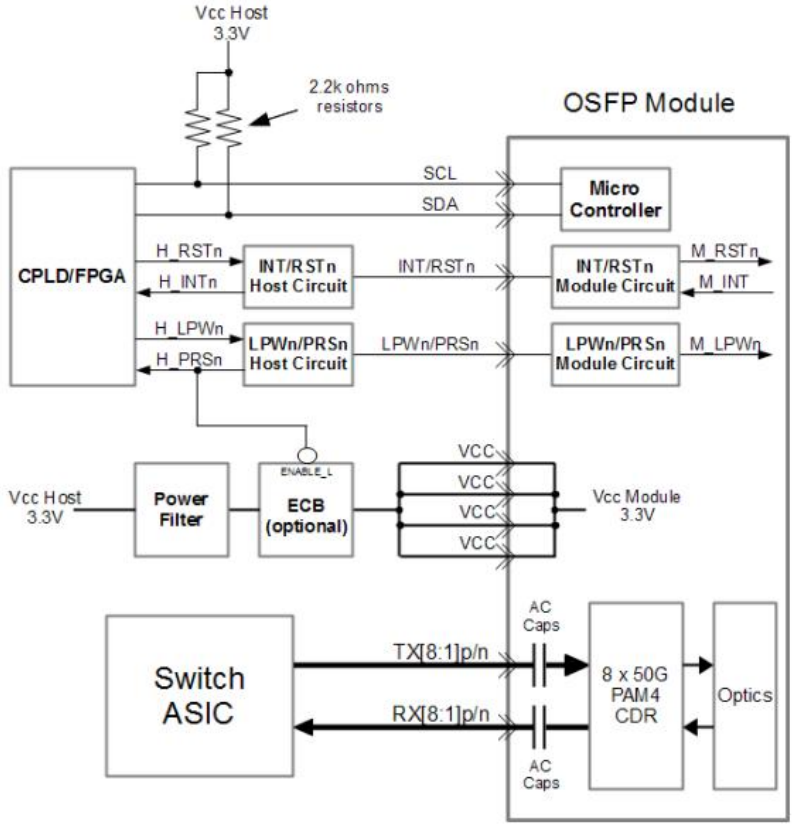


Figure 1, Recommended Interface

## Pin arrangement

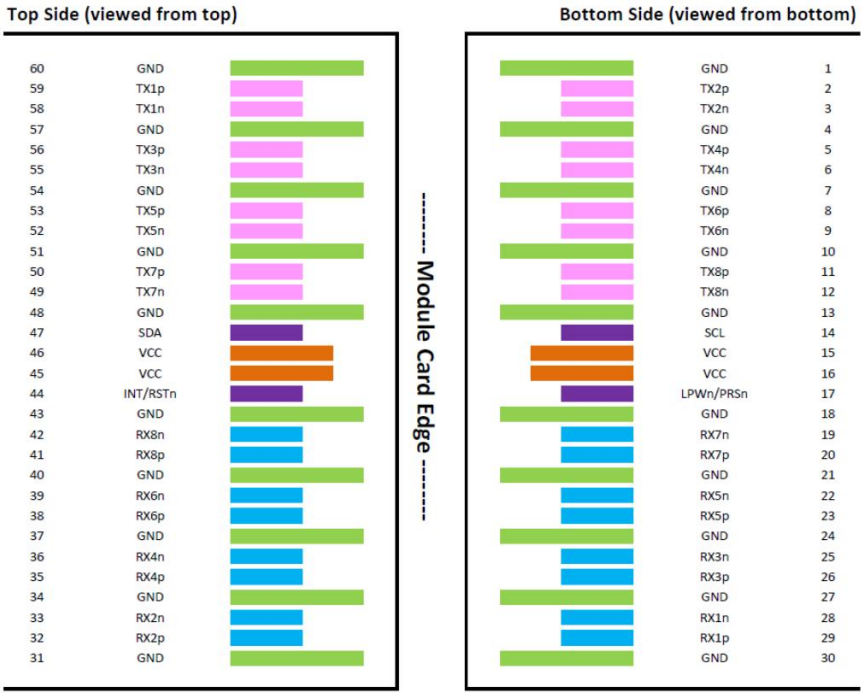


Figure 2, Pin View

## Table 6-Pin Function Definitions

| Pin# | Symbol | Description | Logic | Direction | Plug Sequence | Notes |
|---|---|---|---|---|---|---|
| 1 | GND | Ground | | | 1 | |
| 2 | TX2p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 | |
| 3 | TX2n | Transmitter Data Inverted | CML-I | Input from Host | 3 | |
| 4 | GND | Ground | | | 1 | |
| 5 | TX4p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 | |
| 6 | TX4n | Transmitter Data Inverted | CML-I | Input from Host | 3 | |
| 7 | GND | Ground | | | 1 | |
| 8 | TX6p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 | |
| 9 | TX6n | Transmitter Data Inverted | CML-I | Input from Host | 3 | |
| 10 | GND | Ground | | | 1 | |
| 11 | TX8p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 | |
| 12 | TX8n | Transmitter Data Inverted | CML-I | Input from Host | 3 | |
| 13 | GND | Ground | | | 1 | |
| 14 | SCL | 2-wire Serial interface clock | LVCMOS-I/O | Bi-directional | 3 | Open-Drain with pull-up resistor on Host |
| 15 | VCC | +3.3V Power | | Power from Host | 2 | |
| 16 | VCC | +3.3V Power | | Power from Host | 2 | |
| 17 | LPWn/PRSn | Low-Power Mode / Module Present | Multi-Level | Bi-directional | 3 | See pin description for required circuit |
| 18 | GND | Ground | | | 1 | |
| 19 | RX7n | Receiver Data Inverted | CML-O | Output to Host | 3 | |
| 20 | RX7p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 | |
| 21 | GND | Ground | | | 1 | |
| 22 | RX5n | Receiver Data Inverted | CML-O | Output to Host | 3 | |
| 23 | RX5p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 | |
| 24 | GND | Ground | | | 1 | |
| 25 | RX3n | Receiver Data Inverted | CML-O | Output to Host | 3 | |
| 26 | RX3p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 | |
| 27 | GND | Ground | | | 1 | |
| 28 | RX1n | Receiver Data Inverted | CML-O | Output to Host | 3 | |
| 29 | RX1p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 | |
| 30 | GND | Ground | | | 1 | |

| Pin# | Symbol | Description | Logic | Direction | Plug Sequence | Notes |
|---|---|---|---|---|---|---|
| 31 | GND | Ground | | | 1 | |
| 32 | RX2p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 | |
| 33 | RX2n | Receiver Data Inverted | CML-O | Output to Host | 3 | |
| 34 | GND | Ground | | | 1 | |
| 35 | RX4p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 | |
| 36 | RX4n | Receiver Data Inverted | CML-O | Output to Host | 3 | |
| 37 | GND | Ground | | | 1 | |
| 38 | RX6p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 | |
| 39 | RX6n | Receiver Data Inverted | CML-O | Output to Host | 3 | |
| 40 | GND | Ground | | | 1 | |
| 41 | RX8p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 | |
| 42 | RX8n | Receiver Data Inverted | CML-O | Output to Host | 3 | |
| 43 | GND | Ground | | | 1 | |
| 44 | INT/RSTn | Module Interrupt / Module Reset | Multi-Level | Bi-directional | 3 | See pin description for required circuit |
| 45 | VCC | +3.3V Power | | Power from Host | 2 | |
| 46 | VCC | +3.3V Power | | Power from Host | 2 | |
| 47 | SDA | 2-wire Serial interface data | LVCMOS-I/O | Bi-directional | 3 | Open-Drain with pull-up resistor on Host |
| 48 | GND | Ground | | | 1 | |
| 49 | TX7n | Transmitter Data Inverted | CML-I | Input from Host | 3 | |
| 50 | TX7p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 | |
| 51 | GND | Ground | | | 1 | |
| 52 | TX5n | Transmitter Data Inverted | CML-I | Input from Host | 3 | |
| 53 | TX5p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 | |
| 54 | GND | Ground | | | 1 | |
| 55 | TX3n | Transmitter Data Inverted | CML-I | Input from Host | 3 | |
| 56 | TX3p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 | |
| 57 | GND | Ground | | | 1 | |
| 58 | TX1n | Transmitter Data Inverted | CML-I | Input from Host | 3 | |
| 59 | TX1p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 | |
| 60 | GND | Ground | | | 1 | |

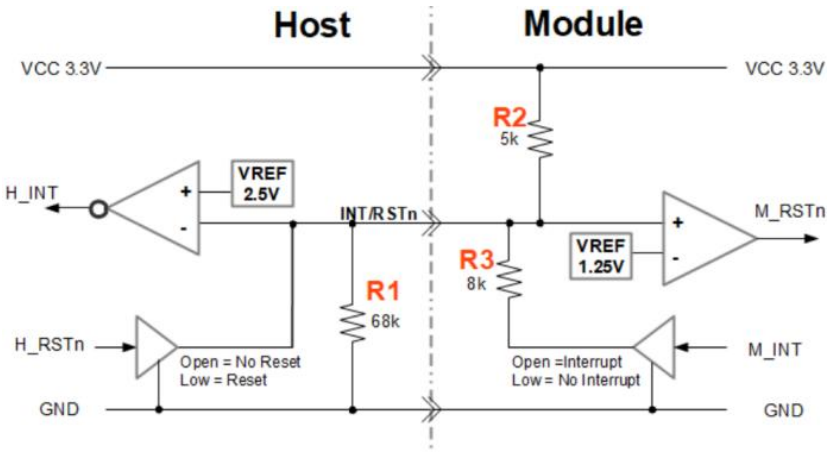


Figure 2, INT/RSTn circuit

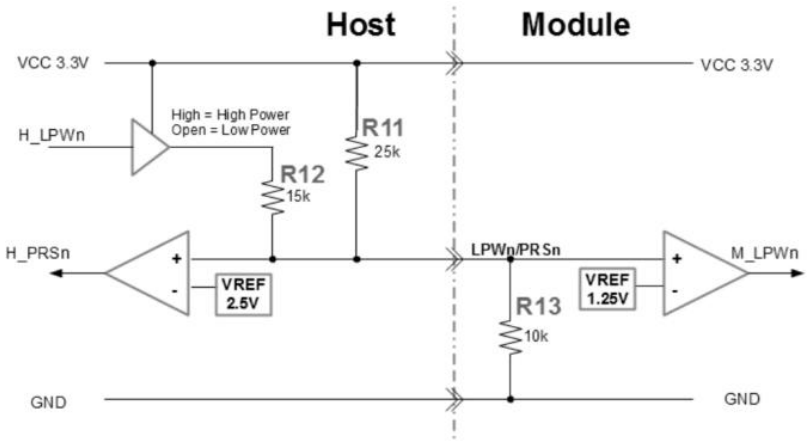


Figure 3, LPWn/PRSn circuit

## Memory Map

Compatible with CMIS rev 5.2.

## Opticalinterface arrangement

The optical port is a male MPO connector receptacle, with fiber lane assignments as shown in Figure 4

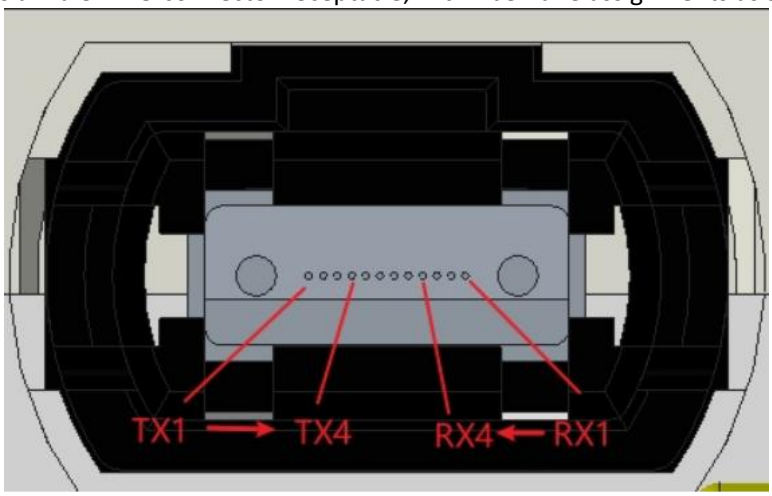


Figure 4,Optical interface arrangement.

## Mechanical

400G SR4 OSFP transceivers are compatible with OSFP MSA Rev 5.0 forOSFP OCTAL SMALL FORM FACTOR PLUGGABLE MODULE.

**Unit mm**

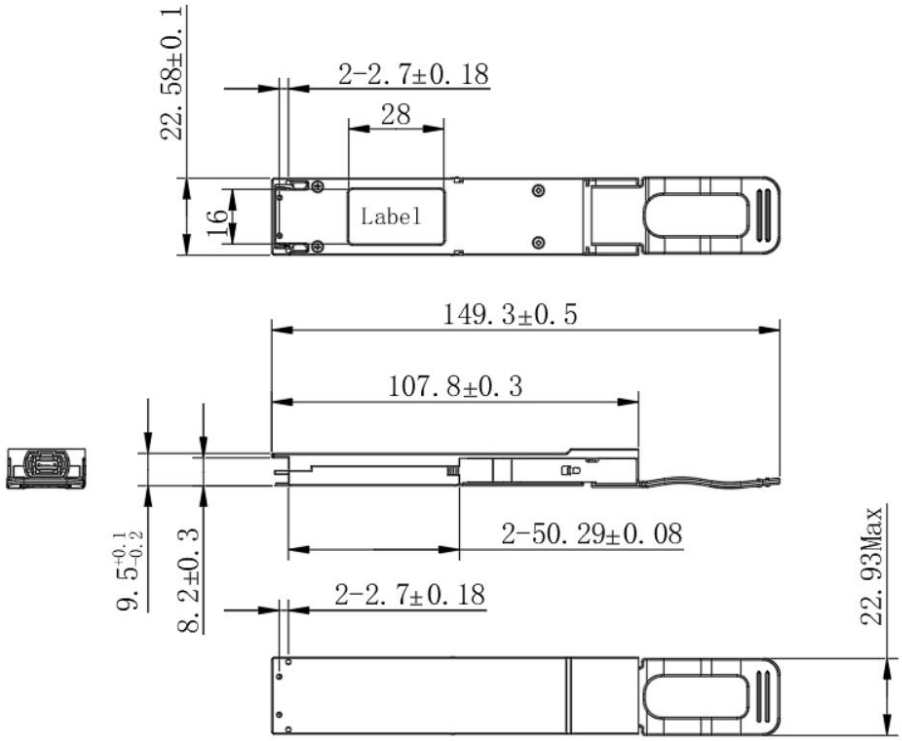


Figure 5,Mechanical Diagram**Warnings**

**Handling Precautions:** This device is susceptible to damage as a result of electrostatic discharge (ESD). A static free environment is highly recommended. Follow guidelines according to proper ESD procedures.

**Laser Safety:** Radiation emitted by laser devices can be dangerous to human eyes. Avoid eye exposure to direct or indirect radiation.