

1.6T OSFP to OSFP Active Optical Cable

Features

- 8x212.5Gbps PAM4 signaling (106.25 GBd) electrical interface
- Integrated 850nm VCSEL array and PD array
- Up to 100m for OM4 fiber
- Power dissipation $\leq 25\text{W}$
- Operating case temperature: 0°C to 70°C
- Built-in digital diagnostic functions
- 3.3V power supply voltage
- RoHS compliant

Standards Compliance

- IEEE802.3ck and IEEE 802.3dj compliant
- OSFP MSA 5.0 and CMIS 5.1 compliant
- OSFP MSA

Applications

- 1600G Ethernet
- HPC Interconnects
- Proprietary Interconnection

General Description

The 1600G OSFP AOC is 1600Gb/s OSFP to 1600Gb/s OSFP InfiniBand NDR Active Optical Cable. Using the Form Factor Pluggable OSFP and contains eight high-speed electrical copper pairs, each operating at data rates of up to 212Gb/s. This cable is compliant with OSFP MSA (Multi-Source Agreement) and IEEE 802.3 standards.

AOCs enable higher port bandwidth, density and configurability at a low cost, and reduced power requirement in the data centers, used extensively in cloud and supercomputers..

Part No.	Specifications					
	Package	Data rate	Wavelength	Temp	Reach	Minimum Bend Radius
VA6R-6RNC100	OSFP-IHS-Close to OSFP-IHS-Close	1700Gbps	$850\pm 10\text{nm}$	$0\sim 70^{\circ}\text{C}$	100m	30mm
VA6R-6RNP100	OSFP-IHS-OPEN to OSFP-IHS-OPEN	1700Gbps	$850\pm 10\text{nm}$	$0\sim 70^{\circ}\text{C}$	100m	30mm

1 Absolute Maximum Ratings and Operation Conditions

Table 1.1 Absolute Maximum Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit
Supply Voltage	Vcc	-0.3	-	3.6	V
Storage Temperature	Ts	-40	-	+85	°C
Operating Humidity	RH	15	-	70	%
Control Input Voltage	VI	-0.3	-	VCC+0.3	V

Table 1.2 Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Case Temperature	TC	0	-	70	°C
Host Bit Rate	BR		106.25		GBd
Number of Lanes		8			
Power Supply Voltage	Vcc	3.135	3.3	3.465	V
Power Dissipation	Pdiss	-	-	25	W
Supply Current	Icc	-	-	7.576	A
Pre-FEC Bit Error Ratio	-	-	2.4e-4	-	
Post-FEC Bit Error Ratio(a)	-	-	1e-12	-	
I2C Clock Frequency			100	400	kHz
Logic Input Voltage High	Vih	V	2		Vcc+0.3
Logic Input Voltage Low	Vil	V	-0.3		0.8

Note: a. PRBS31Q test pattern is used & FEC provided by host system.

2 OSFP Parameters

2.1 OSFP Electrical Pin Assignment

The OSFP module is based on a 60 pin electrical connector with pin out as specified in OSFP Hardware specification. The 60 electrical pins allow exchanging high speed data, control and alarm signals between module and host board. The pin-outs are summarized below:

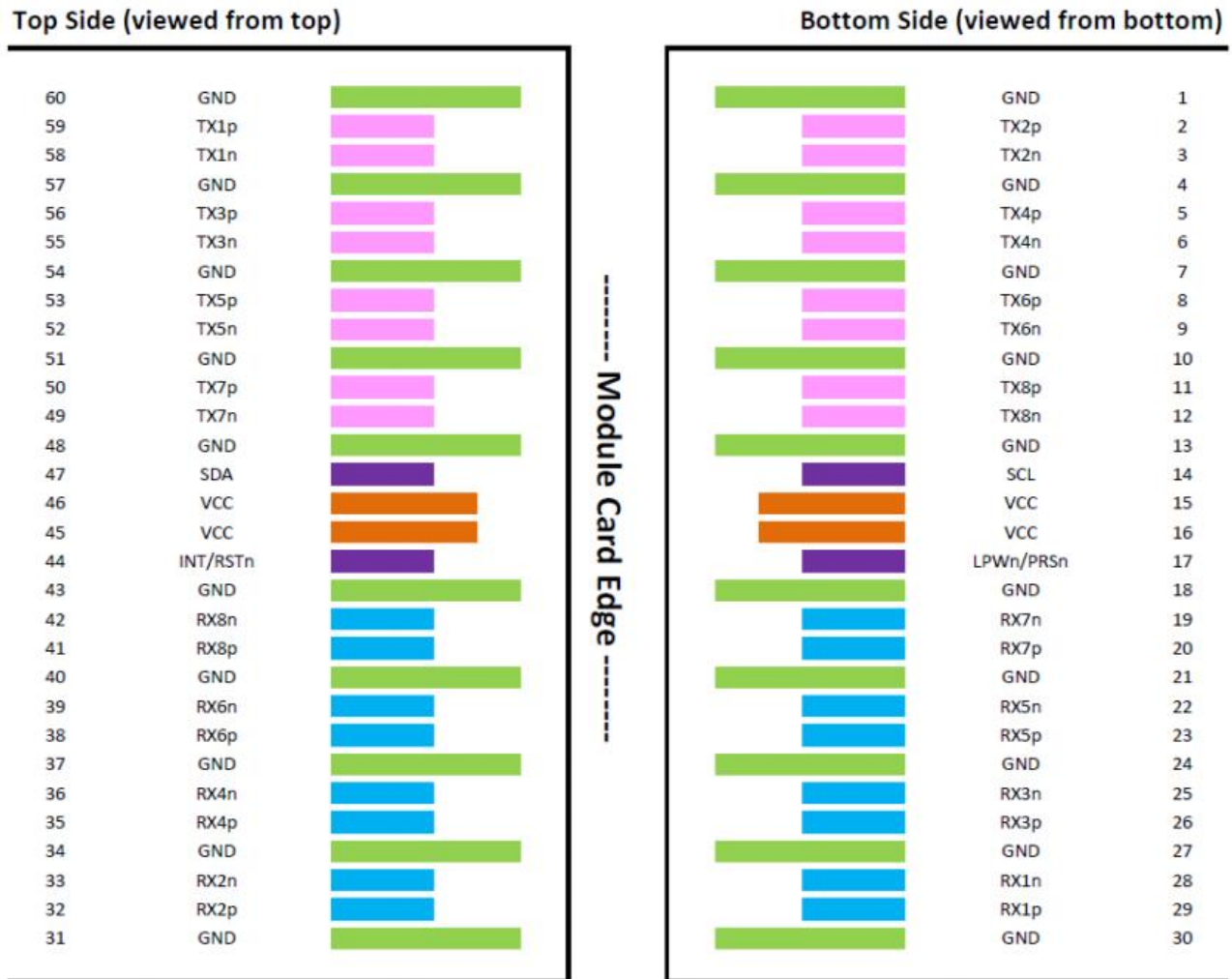


Figure 2.1 OSFP module pinout

Pad#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
1	GND	Ground				
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	nput from Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	nput from Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground			1	
8	TX6p	Transmitter Data Non-Inverted	CML-I	nput from Host	3	
9	TX6n	Transmitter Data Inverted	CML-I	nput from Host	3	
10	GND	Grounc			1	
11	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX6n	Transmitter Data Inverted	CML-I	nput from Host	3	
13	GND	Ground				
14	SCL	2-wire serial interface clock	LVC MOS-VO	Bi-directional	3	Open-Drain with pull-up resistor on Host
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/PRSn	Low-Power Mode/Module Present	Multi-Level	Bi-directional	3	See pin description for required circuit
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground				
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
27	GND	Ground				
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	

29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
30	GND	Ground				
31	GND	Ground				
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3	
40	GND	Ground				
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3	
43	GND	Ground				
44	INT/RSTn	Module Interrupt/Module Reset	Multi-Level	Bi-directional	3	See pin description for required circuit
45	VCC	+3.3V Power		Power from Host	2	
46	VCC	+3.3V Power		Power from Host	2	
47	SDA	2-wire serial interface Data	LVC MOS-VO	Bi-directional	3	Open-Drain with pull-up resistor on Host
48	GND	Ground				
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3	
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
51	GND	Ground				
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3	
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
54	GND	Ground				
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3	
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground				

58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-1	Input from Host	3	
60	GND	Ground				

2.2 OSFP Electric Ports Definition

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Transmitter						
Signaling Rate,each Lane	-	Gbaud	106.25±100 ppm			
Modulation Format	-	-	PAM4			
Differential Input Voltage Amplitude	V _{in} ,ppd	mV	650	-	800	
Differential Termination Mismatch	-	%	-	-	10	
DC Common-mode Voltage Tolerance	-	mV	350	-	2850	
Receiver						
Signaling Rate,each Lane	-	Gbaud	106.25±100 ppm			
Modulation Format	-	-	PAM4			
Differential Output Voltage (Long mode)	V _{out} ,ppd	mV	-	-	845	
Differential Output Voltage (Short mode)	V _{out} ,ppd	mV	-	-	600	
Differential Termination Mismatch	-	%	-	-	10	
DC Common-mode Voltage Tolerance	-	mV	-350	-	2850	

2.3 Module Memory Map

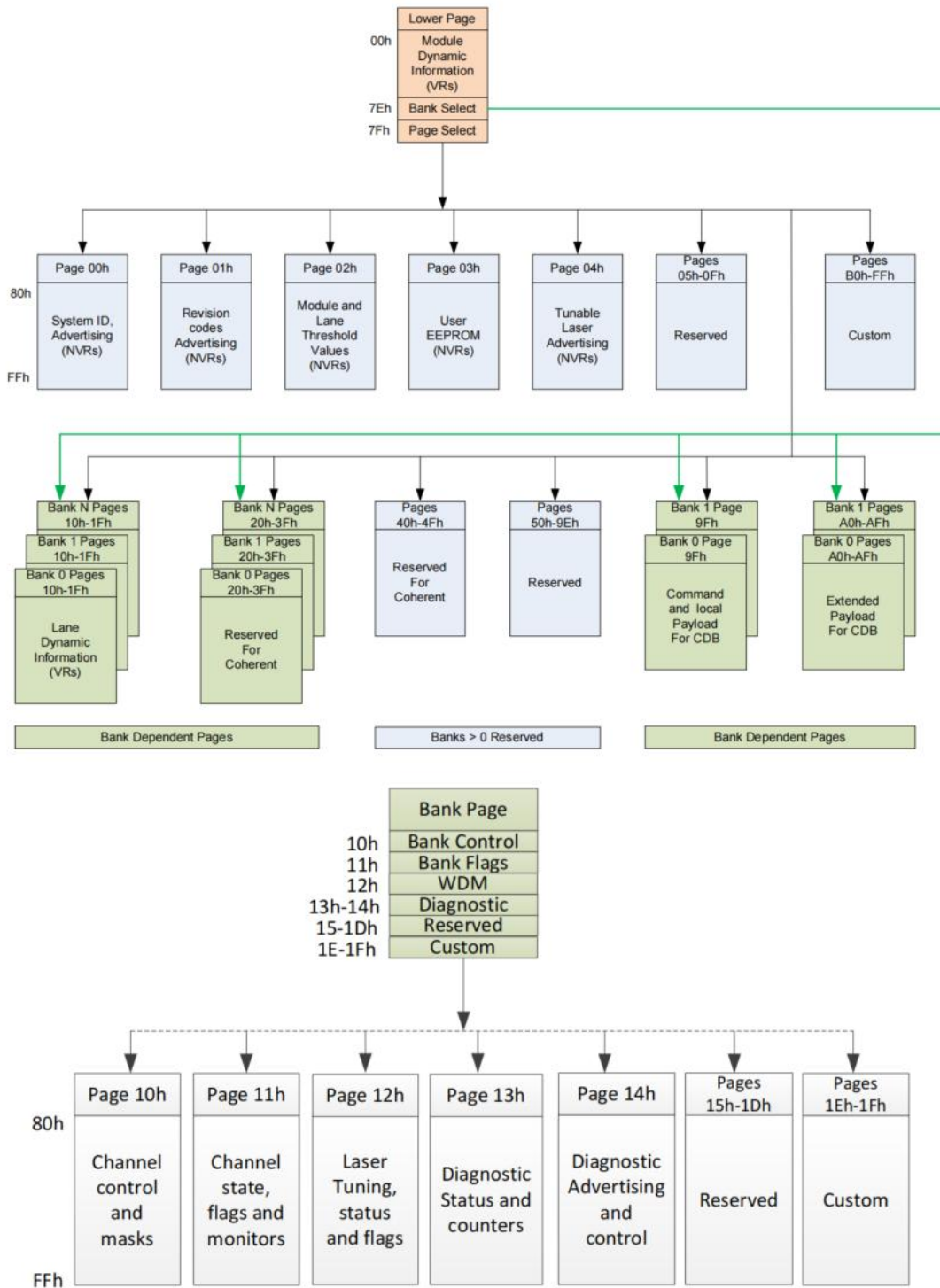


Figure 2.2 Digital Diagnostic Memory Map

3 Environment Regulation Compliance and product Safety

Category	Standard
Radiated Emissions	EN 55032 Class B CISPR 32 Class B FCC rules 47 CFR Part15
Radiated Immunity	EN 55035 CISPR 35 IEC/EN 61000-4-3
RoHS	EU RoHS 2.0 (2011/65/EU) REACH (EC 1907/2006) China RoHS SJ/T 11363
Laser Safety	IEC 60825-1:2014+A11:2021 FDA/CDRH Class 1 Laser Product, 21 CFR 1040.10 & 1040.11
ESD	IEC 61000-4-2; ANSI/ESDA/JEDEC JS-001; MIL-STD-883C Contact $\pm 8\text{kV}$, Air $\pm 15\text{kV}$
Flammability (PCB)	UL Class 94 V-0
Reliability	GR-468-CORE、IEC 61300-2

4 Important Notice

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5 Revision History

Revision	Date	Description
V1.0	2026.4.9	Advance Release.