800G OSFP 2xVR4 Optical Transceiver

Features

- Dual MPO-12/APC optical connectors
- Support 2x425Gb/s aggregate bit rate
- Up to 50m over MMF
- Power dissipation < 16W
- Operating case temperature: 0°C to 70°C
- Built-in digital diagnostic functions
- 3.3V power supply voltage
- RoHS compliant

Standards Compliance

- IEEE802.3db and IEEE 802.3ck compliant
- OSFP MSA 5.0 and CMIS 5.2 compliant

Applications

- InfiniBand NDR
- 800G VR8 application with FEC
- 2x400G VR4 application with FEC
- 8 x 100GbE breakout applications

General Description

The 800G OSFP 2xVR4 transceiver module is designed for 800 Gigabit Ethernet links over 30 m on OM3 or 50 m on OM4 multimode fiber (MMF). The module features 8 independent electrical input/output channels operating at 106.25 Gbps (PAM4 modulation), and 8 optical lanes each transmitting at 100 Gbps for an aggregate data rate of 800 Gbps. The module is compliant with the OSFP MSA form factor and supports the 800GAUI-8 electrical interface (8 × 106.25 Gbps). The optical interface utilizes a dual MPO-12 connector assembly with 16 active fibers (8 transmit and 8 receive), enabling parallel transmission over 8 optical lanes. The module is designed to operate over the commercial temperature range of 0°C to +70°C and supports Digital Diagnostic Monitoring (DDM) functions via the I²C management interface in accordance with CMIS 5.2.

Part No.	Specifications					
	Package	Data rate	Wavelength	Temp	Reach	Optical Interface
VD5Q0-J085R	OSFP112	850Gbps	850nm	0~70℃	50m	2*MPO12

1 Absolute Maximum Ratings and Operation Conditions

Table 1.1 Absolute Maximum Ratings

Parameter	Symbol	Unit	Min	Max
Supply Voltage	V_{CC}	V	-0.5	3.6
Storage Temperature	Tsto	°C	-40	85
RelativeHumidity (Non-condensing)	RH	%	5	95
Control Input Voltage	V_i	V	-0.3	V_{CC}+0.5

Table 1.2 Operating Conditions

Parameter	Symbol	Unit	Min	Typ	Max	NOTE
Power Supply Voltage	V_{CC}	V	3.135	3.3	3.465	
Case Operating Temperature	Top	°C	0		70	
Relative Humidity (Non-condensing)	RH	%	15		85	
I2C Clock Frequency		kHz		100	400	

2 OSFP Parameters

2.1 OSFP Electrical Pin Assignment

The OSFP module is based on a 60 pin electrical connector with pin out as specified in OSFP Hardware specification. The 60 electrical pins allow exchanging high speed data, control and alarm signals between module and host board. The pin-outs are summarized below：

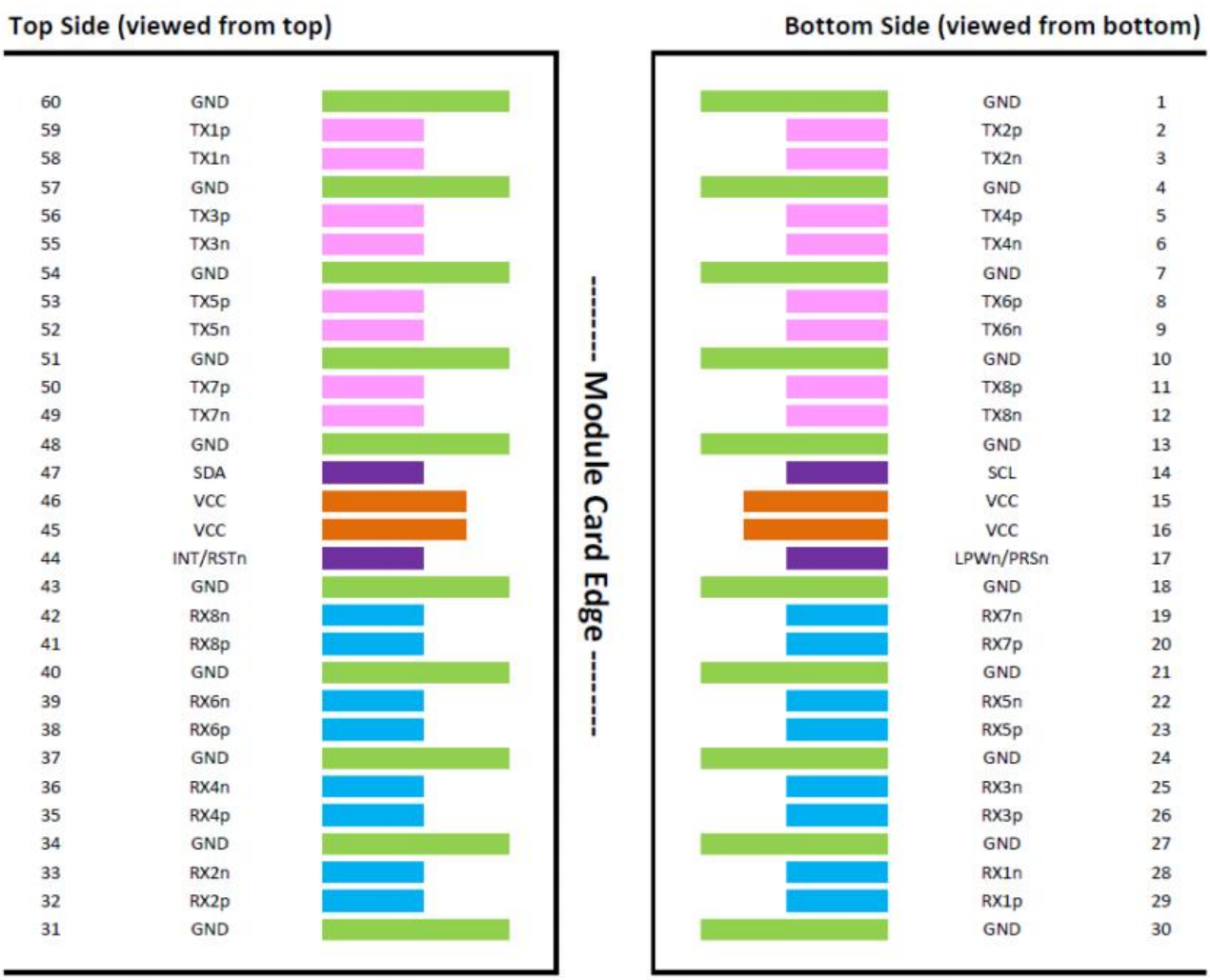

Figure 2.1 OSFP module pinout

Pad#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
1	GND	Ground				
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	nput from Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	nput from Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground			1	
8	TX6p	Transmitter Data Non-Inverted	CML-I	nput from Host	3	
9	TX6n	Transmitter Data Irverted	CML-I	nput from Host	3	
10	GND	Grounc			1	
11	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX6n	Transmitter Data Inverted	CML-I	nput from Host	3	
13	GND	Ground				
14	SCL	2-wire serial interface clock	LVCMOS-VO	Bi-directional	3	Open-Drain with pull-up resistor on Host
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/PRSn	Low-Power Mode/Module Present	Multi-Level	Bi-directional	3	See pin description for reguired circ uit
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground				
22	RX5n	Receiver Data Irverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Irverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
27	GND	Ground				

28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
30	GND	Ground				
31	GND	Ground				
32	RX2p	Receiver Data Non-Irverted	CML-O	Output to Host	3	
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Irverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
39	RX6n	Receiver Data Irverted	CML-O	Output to Host	3	
40	GND	Ground				
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3	
43	GND	Ground				
44	INT/RSTn	Module Interrupt/Module Reset	Multi-Level	Bi-directional	3	See pin description for required circuit
45	VCC	+3.3V Power		Power from Host	2	
46	VCC	+3.3V Power		Power from Host	2	
47	SDA	2-wire serial interface Data	LVCMOS-VO	Bi-directional	3	Open-Drain with pull-up resistor on Host
48	GND	Ground				
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3	
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
51	GND	Ground				
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3	
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
54	GND	Ground				
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3	

56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground				
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-1	Input from Host	3	
60	GND	Ground				

2.2 OSFP Electric Ports Definition

Parameter	Symbol	Unit	Min	Typ	Max	Note
Power Supply Current	Icc	mA			5000	
Power On Initialization Time	Tinit	ms			2000	
Transmitter						
Signaling Speed, each lane		GBd		53.125		
Signaling Speed Tolerance		ppm	-100		+100	
Differential pk-pk input voltage tolerance	Vin,pp	mV	750			
Peak-to-peak AC common-mode voltage tolerance Low-frequency, VCMLF Full-band, VCMFB		mV	 32 80			
Differential Input Impedance	Zin	Ohms	90	100	110	
Effective return loss	ERL	dB	8.5			
Single-ended voltage tolerance range		V	-0.4		3.3	
DC Common Mode Voltage		V	-0.35		2.85	
Receiver						
Signaling Speed, each lane		GBd		53.125		
Signaling Speed Tolerance		ppm	-100		+100	
Peak-to-peak AC common-mode voltage Low-frequency, VCMLF Full-band, VCMFB		mV			 32 80	
Differential pk-pk output voltage Short mode Long mode Disabled	Vout,pp	mV			 600 845 35	
Eye Height	EH	mV	15			
Vertical eye closure, VEC		dB			12	

Differential Output Impedance	Zout	Ohms	90	100	110	
Transition Time, 20% to 80%	Tr, Tf	ps	8.5			
DC Common Mode Voltage		V	-0.35		2.85	

2.3 Optical Characteristics

Parameter	Symbol	Unit	Min	Typ	Max	Note
Transmitter						
Signaling Speed		GBd		53.125		
Signaling Speed Tolerance		ppm	-100		+100	
Modulation Format		PAM4				
Lane Wavelength		nm	844	850	870	
RMS Spectral Width	SW	nm			0.65	1
Average TX Power	Pavg	dBm	-4.6		4	2
Outer Optical Modulation Amplitude for TDECQ < 1.8dB for 1.8dB ≤ TDECQ ≤ 4.4dB	OMAouter	dBm	-2.6 -4.4+max(TECQ,TDECQ)		3.5	
Extinction Ratio	ER	dB	2.5			
Average launch power of OFF transmitter, each lane	Poff	dBm			-30	
Transmitter and dispersion eye closure for PAM4	TDECQ	dB			4.4	
Transmitter eye closure for PAM4	TECQ	dB			4.4	
Transmitter overshoot and undershoot		%			29	
Transmitter power excursion		dBm			2.3	
Transmitter transition time		ps			17	
Relative Intensity Noise	RIN	dB/Hz			-132	
Optical return loss tolerance	ORTL	dB			18	

Encircled flux		dBm	≥86% at 19µm ≤30% at 4.5µm			2
Receiver						
Signaling Speed		GBd		53.125		
Signaling Speed Tolerance			-100		+100	
Modulation Format		PAM4				
Lane Wavelength			842	850	948	
Damage Threshold			5			3
Average RX Power		dBm	-6.4		4	4
RX Power (OMA_{outer})		dBm			3.5	
RX Reflectance		dBm			-15	
RX Sensitivity (OMA_{outer})		dBm			Max(-4.6, -6.2+TECQ)	
Stressed receiver sensitivity (OMA_{outer}) (max)		dBm			-1.8	5
Conditions of stressed receiver sensitivity test						6
OMA_{outer} of Each Agressor Lane		dBm	3.5			
Stressed eye closure for PAM4 (SECQ), lane under test		dB	4.4			

Notes:

1. RMS spectral width is the standard deviation of the spectrum.
2. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance
3. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power
4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance
5. Measured with conformance test signal at TP3 for the BER specified in 167.1.1.
6. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

2.3 Digital Diagnostic Functions

Parameter	Symbol	Min	Max	Units	Notes

Temperature monitor absolute error	DMI_Temp	-3	3	℃	Over operating temperature range
Supply voltage monitor absolute error	DMI _VCC	-0.1	0.1	V	Over full operating range
Channel RX power monitor absolute error	DMI_RX_Ch	-2	2	dB	
Channel Bias current monitor	DMI_Ibias_Ch	-10%	10%	mA	
Channel TX power monitor absolute error	DMI_TX_Ch	-2	2	dB	

2.4 Recommended Power Supply Filter

Figure 2.2 provides an example implementation for a 3.3V power filter on the host board. If an alternate circuit is used for power filtering then the same filter characteristics as this example filter shall be met.

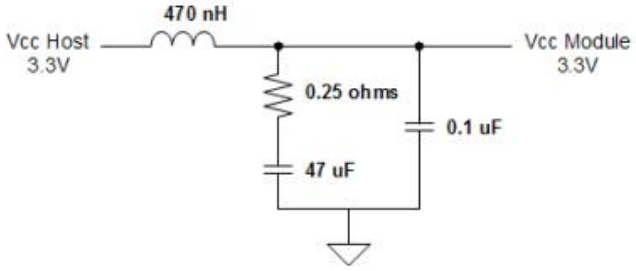

Figure 2.2 Recommended Host Board Power Supply Filtering

2.5 OSFP Host Board and Module Block Diagram

Figure 2.3 is an example block diagram of the host board's connections to the OSFP module.

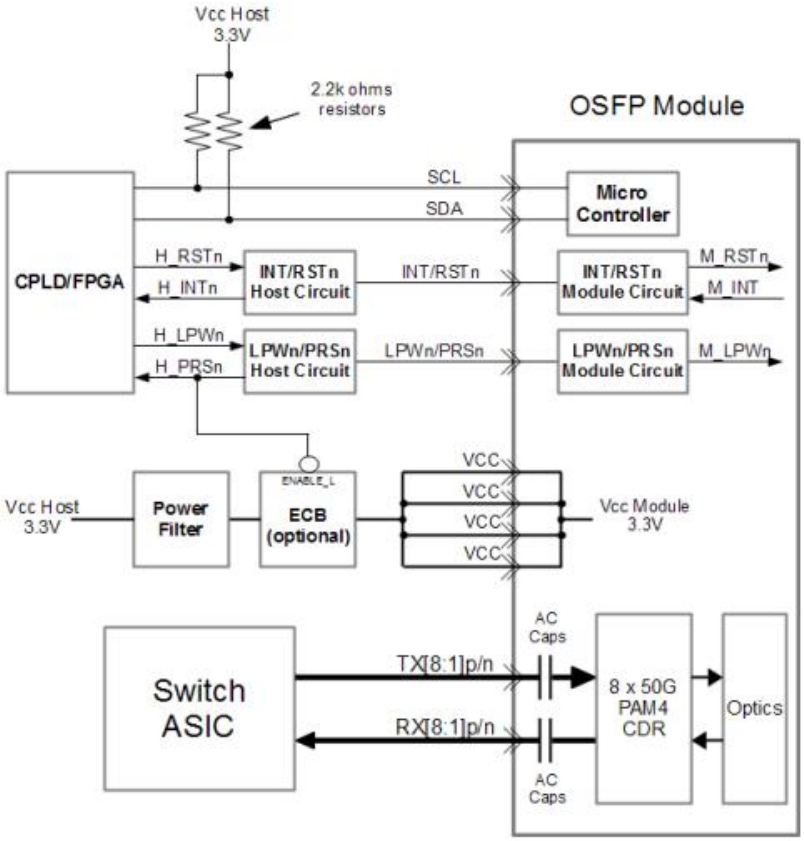

Figure 2.3 OSFP Host Board and Module Block Diagram

2.6 Module Memory Map

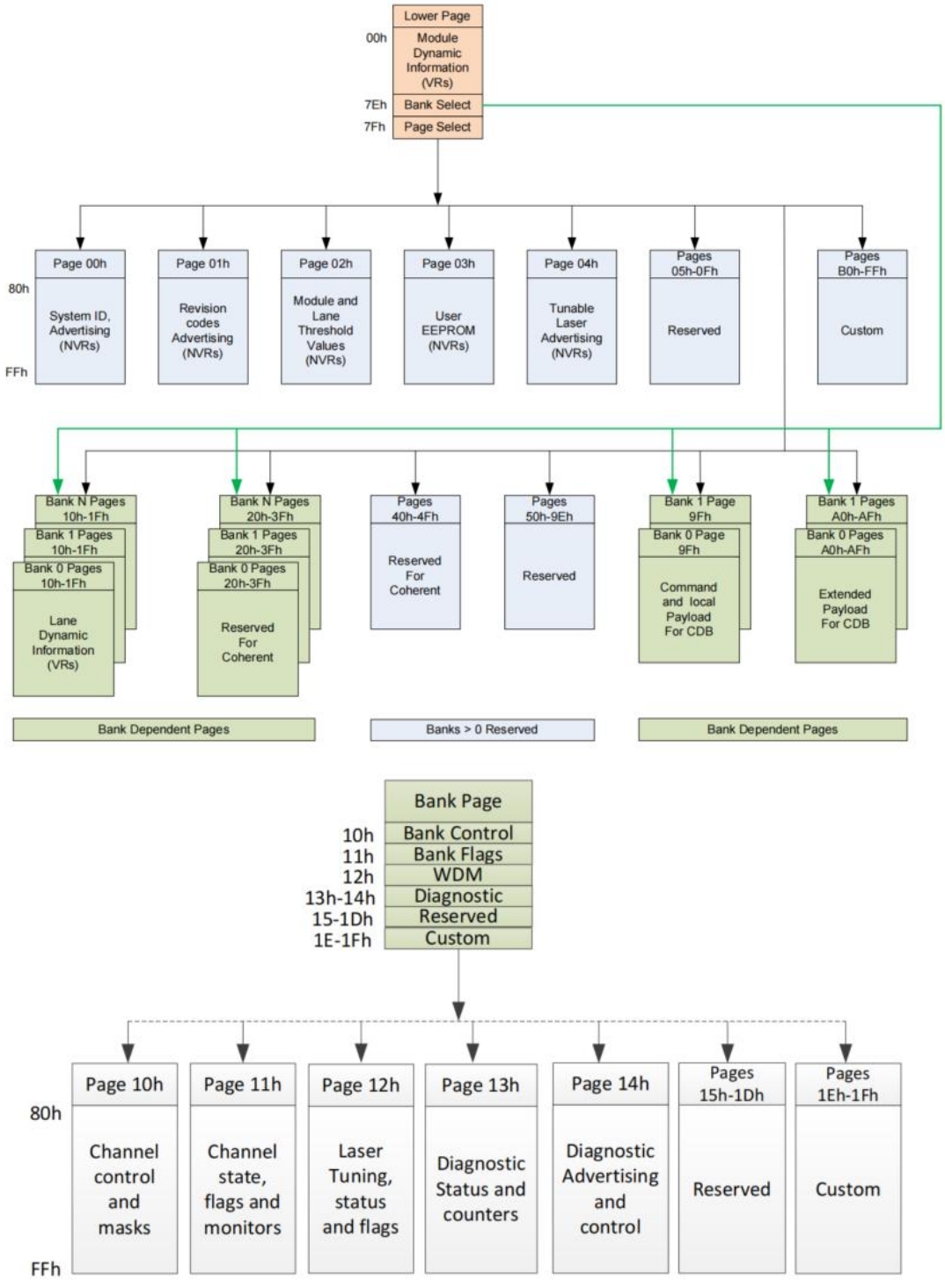

Figure 2.4 Digital Diagnostic Memory Map

3 Environment Regulation Compliance and product Safety

Category	Standard
Radiated Emissions	EN 55032 Class B CISPR 32 Class B FCC rules 47 CFR Part15
Radiated Immunity	EN 55035 CISPR 35 IEC/EN 61000-4-3
RoHS	EU RoHS 2.0 (2011/65/EU) REACH (EC 1907/2006) China RoHS SJ/T 11363
Laser Safety	IEC 60825-1:2014+A11:2021 FDA/CDRH Class 1 Laser Product, 21 CFR 1040.10 & 1040.11
ESD	IEC 61000-4-2；ANSI/ESDA/JEDEC JS-001；MIL-STD-883C Contact ±8kV, Air ±15kV
Flammability (PCB)	UL Class 94 V-0
Reliability	GR-468-CORE、IEC 61300-2

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5 Revision History

Revision	Date	Description
V1.0	2025.12.20	Advance Release.