

800G OSFP To 2*400G OSFP-Finned Active Electrical Cable

Features

- Support I2C two - line string interface
- Support 112G (PAM4) electrical data rates Support for hot plugging
- 3.3V power supply
- Power consumption: 10W, per 800G end
- Power consumption 7W, per 400G end
- Maximum Link Length: up to 7m
- Operating case temperature: 0~70°C
- RoHS Compliance

Standards Compliance

- Compliant with OSFP MSA
- Compliant with IEEE802.3ck
- Compliant with CMIS 5.1

Applications

- Switches
- Routers
- Data center, server
- InfiniBand NDR/HDR/EDR
- 800G/400G Ethernet

General Description

The VE5Q-4QDGxxx is designed for use in 800G/400G Ethernet. OSFP is the module and cage/connector system based on current OSFP, targeting to support the 112Gb/s per lane speed in a 8&4 lane OSFP system and to enable the OSFP 800G&400G interconnect ecosystem.

Part No.	Package	Conductor Size	Length	Temp
VE5Q-4QDG007	OSFP-Finned to 2*OSFP-RHS	28AWG	7M	0~70°C

1 Absolute Maximum Ratings and Operation Conditions

Table 1.1 Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ	Max.	Unit
Supply Voltage	Vcc	-0.5	-	3.6	V
Storage Temperature	Ts	-40	-	+85	°C
Operating Humidity	RH	5	-	+85	%

Table 1.2 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating Case Temperature(note1)	TC	0	-	70	°C
Power Supply Voltage	Vcc	3.135	3.3	3.465	V
Power Dissipation(800G, per end)	Pdiss	-	-	10	W
Power Dissipation(400G, per end)	Pdiss	-	-	7	W
Pre-FEC Bit Error Ratio(PRBS31Q)	-	-	1e-8		-
Post-FEC Bit Error Ratio(PRBS31Q)	-	-	1e-15		-
Data Rate per Lane			53.125		Gbd

Notes: 1, The temperature tolerance

2 OSFP Parameters

2.1 OSFP Electrical Pin Assignment

The OSFP module is based on a 60 pin electrical connector with pin out as specified in OSFP Hardware specification. The 60 electrical pins allow exchanging high speed data, control and alarm signals between module and host board. The pin-outs are summarized below:

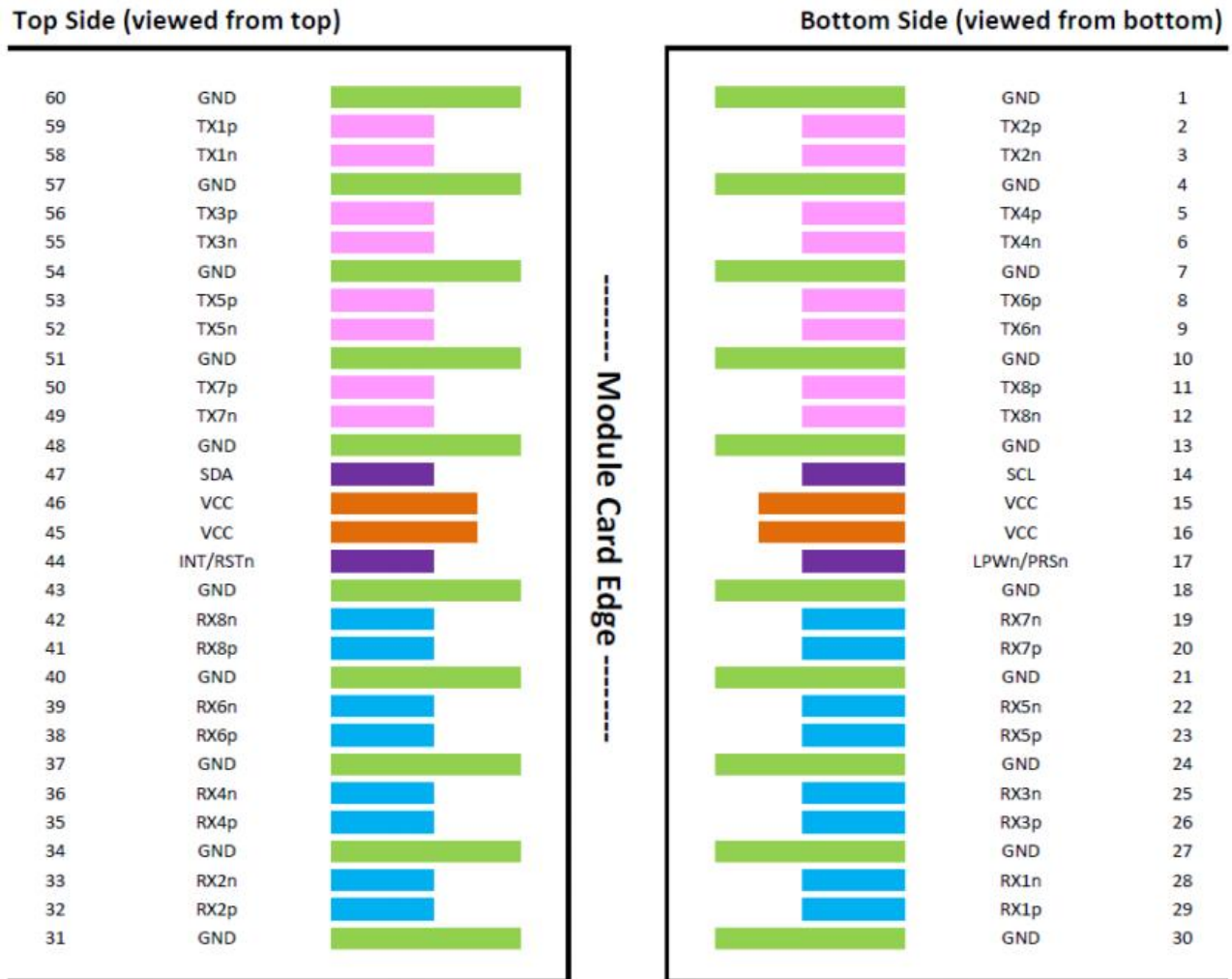


Figure 2.1 OSFP module pinout

Pad#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
1	GND	Ground				
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	nput from Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	nput from Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground			1	
8	TX6p	Transmitter Data Non-Inverted	CML-I	nput from Host	3	
9	TX6n	Transmitter Data Inverted	CML-I	nput from Host	3	
10	GND	Grounc			1	
11	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX6n	Transmitter Data Inverted	CML-I	nput from Host	3	
13	GND	Ground				
14	SCL	2-wire serial interface clock	LVC MOS-VO	Bi-directional	3	Open-Drain with pull-up resistor on Host
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/PRSn	Low-Power Mode/Module Present	Multi-Level	Bi-directional	3	See pin description for required circuit
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	

21	GND	Ground				
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
27	GND	Ground				
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
30	GND	Ground				
31	GND	Ground				
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3	
40	GND	Ground				
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3	
43	GND	Ground				
44	INT/RSTn	Module Interrupt/Module Reset	Multi-Level	Bi-directional	3	See pin description for

						required circuit
45	VCC	+3.3V Power		Power from Host	2	
46	VCC	+3.3V Power		Power from Host	2	
47	SDA	2-wire serial interface Data	LVC MOS-VO	Bi-directional	3	Open-Drain with pull-up resistor on Host
48	GND	Ground				
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3	
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
51	GND	Ground				
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3	
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
54	GND	Ground				
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3	
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground				
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-1	Input from Host	3	
60	GND	Ground				

3 Important Notice

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4 Revision History

Revision	Date	Description
V1.0	2026.4.10	Advance Release.